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10/823,658	04/14/2004	Kohei Oikawa	251862US2S	4967

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EXAMINER	
RIZK, SAMIR WADIE	

ART UNIT	PAPER NUMBER
2112	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/823,658	OIKAWA, KOHEI	
	Examiner	Art Unit	
	Sam Rizk	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 March 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7-14 and 18-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-14 and 18-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

- Response to the applicant's amendment dated 3/12/2007
- Claims 6 and 15-17 have been Cancelled
- Amended claims 1-5 and 7-14 have been submitted for examination
- New claims 18-20 have been submitted for examination
- Claims 1-5, 7-14 and 18-20 have been rejected

Response to Arguments

1. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies: For example, applicant argument in page 6, lines 20-24, filed on 3/12/2007 recites (emphasis added):

"More specifically, and with reference to Figure 1 in the present specification as a non-limiting example, the claimed invention can operate to **(a) divide data during a writing operation**, for example dividing 32-bit cell data (input/output data) **into first 19-bit data that includes 6-bit parity data** and second 19-bit data that does not include parity bits,."

are not recited in the rejected claims. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

2. In response to applicant's other arguments with respect to the amended claim 1 that the memory cell array includes a first area and a second area, and parity data is written into the first area the have been considered and are persuasive.

Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Hogashitani et al. US patent no. 5671239 (Hereinafter Hogashitani) and in further view of Shinoda et al. US patent no. 4817052 (Hereinafter Shinoda).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1-5,7-17 and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hogashitani and in further view of Shinoda.

4. In regard to claim 1,

Claim 1 (Currently Amended): A semiconductor memory device comprising:

- a memory cell array including at least a first area (M-ARY1 in FIG. 1 in Shinoda) and a second area (M-ARY2 in FIG. 1 in Shinoda), a data

input circuit located closer to the first area than the second area, to which cell data is input (DOB in FIG. 1 in Shinoda);

- an error correction circuit which generates parity data for error correction from the cell data input to the data input circuit; and

(Note: FIG.1, reference character DOB" in Shinoda)

However, Shinoda does not teach:

- a control circuit which writes the parity data into the first area and writes the cell data into the second area at a time of a writing operation stores the parity data in the first area.

Hogashitani in an analogous art that teach semiconductor memory of xN type having parity corresponding to NxM bits teaches:

- a control circuit which writes the parity data into the first area and writes the cell data into the second area at a time of a writing operation stores the parity data in the first area.

(Note: FIG. 2, reference character (6) and col. 5, lines (43-48) and the Abstract, lines (7-9) in Higashitani)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Hogashitani that comprise of separate parity cell block (array) and data cell block (array) with the teaching of Shinoda.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would

have recognized the need to improve the function of the built-in ECC in a memory fabrication.

5. In regard to claim 2, Shinoda teaches:

The semiconductor memory device according to claim 1, wherein the memory array includes a first memory unit and a second memory unit having the first area and the second area, respectively.

(Note: FIG.1, reference characters (M-ART1, M-ARY2) and (M-ARY3, M-ARY4) in Shinoda)

6. In regard to claim 3, Shinoda teaches:

The semiconductor memory device according to claim 1, wherein the memory array includes a first data line connected to the first area and a second data line connected to the second area.

(Note: FIG. 1, the address lines connected to the Y DECODER and the (X DECODER(S) and the SENSE AMPLIFIER(S)

7. In regard to claim 4, Shinoda teaches:

The semiconductor memory device according to claim 3, further comprising a switch between the first data line and the second data line.

(Note: FIG. 1, reference characters (MPXI-MXP4 in Shinoda)

8. In regard to claim 5; Shinoda teaches:

The semiconductor memory device according to claim 1, wherein the memory array includes a common data line connected to both the first area and the

second area.

(Note: FIG. 1, output lines from the X DECODER(S))

9. In regard to claim 7, Shinoda teaches:

The semiconductor memory device according to claim 1, wherein the control circuit stores both the parity data and the cell data in the first area and stores the cell data not including the parity data in the second area.

(Note: FIG. 5 and col.'s 15-18, (TABLE 3) in Shinoda)

10. Claim 8 is rejected for the same reasons as per claim 2.

11. In regard to claim 9, Shinoda teaches:

The semiconductor memory device according to claim 8, wherein the first memory unit has a first data line connected to the first area and a second data line connected to the second area, and the second memory unit has a first data line connected to the first area and a second data line connected to the second area.

(Note: FIG. 1, the address lines connected to the Y DECODER and the (X DECODER(S) and the SENSE AMPLIFIER(S))

12. Claim 10 is rejected for the same reasons as per claim 4.

13. Claim 11 is rejected for the same reasons as per claim 5.

14. In regard to claim 12, Shinoda teaches:

The semiconductor memory device according to claim 1, wherein the memory array includes at least a first memory unit and a second

memory unit each having the first area and the second area, and the semiconductor memory device further comprises a switching circuit which stores the parity data in the first area of one of the first memory unit and the second memory unit.

(Note: FIG. 5 and col.'s 15-18, (TABLE 3) in Shinoda)

15. In regard to claim 13, Shinoda teaches:

The semiconductor memory device according to claim 1, further comprising a data compensating circuit which error-corrects the cell data stored in the memory array using the parity data stored in the first area.

(Note: FIG. 5. in Shinoda)

16. In regard to claim 14, Shinoda teaches:

The semiconductor memory device according to claim 1, wherein a size of the first area is equal to or smaller than that of the second area.

(Note: FIG. 1, reference characters (M-ARY1)-(M-ARY4) in Shinoda)

17. In regard to claim 18, Higashitani teaches:

Claim 18 (New): The semiconductor memory device according to claim 1, wherein the control circuit simultaneously activates the first area and the second area.

(Note: col. 3, lines (49-54) in Higashitani)

18. Claims 19 and 20 are rejected for the same reasons as per claim 12.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sam Rizk whose telephone number is (571) 272-8191. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on (571) 272-6962. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronics Business Center (EBC) at 866-217-9197 (toll-free)

Sam Rizk,

Examiner

ART UNIT 2112

5/22/07

GUY LAMARRE
PRIMARY EXAMINER